AMENDMENTS TO THE CLAIMS

1. (Currently amended) A circuit for dividing periodic input pulses by a preset integer M, comprising:

a dual modulus prescaler arranged to receive periodic input pulses and to count the received input pulses for generating prescaled pulses, wherein one prescaled pulse is generated for every Qth input pulse, wherein Q is a division modulus having a value depending on a value of a modulus control signal, wherein when a prescaled pulse is generated from a selected input pulse, the modulus control signal is ignored at least until after the onset of a next input pulse is received;

a swallow counter arranged to change the modulus control signal to a different value in response to the prescaler receiving every Mth input pulse, wherein M is a preset integer; and

a program counter to generate a reset signal in response to the prescaler receiving the Mth input pulse, and

wherein the swallow counter changes the modulus control signal in response to the reset signal.

2. (Original) The circuit of claim 1, wherein

if the ignored modulus control signal acquires a different value due to the selected input pulse, the next pulse is counted according to a correspondingly different value of Q.

3. (Original) The circuit of claim 2, wherein

when the prescaler receives a selected one of the Mth pulses, the modulus control signal changes value after the prescaler has already received the onset of a next input pulse.

4. (Original) The circuit of claim 1, wherein

the prescaler includes an OR gate for ORing the modulus control signal with another signal.

Claim 5 (canceled)

6. (Previously Presented) The circuit of claim 1, further comprising:

a frequency/phase detector arranged to receive a divided down signal generated in response to the prescaler receiving the Mth input pulse, and to output a synchronized signal in response to the divided down signal; and

a fast clock generator to generate a fast clock signal from the synchronized signal, and wherein the input pulses are derived from the fast clock signal.

7. (Previously Presented) The circuit of claim 1, wherein

the program counter is adapted to generate the reset signal in response to receiving a prescaled pulse that corresponds to the prescaler receiving the Mth input pulse.

8. (Original) The circuit of claim 7, wherein

the prescaler includes components that define state variables which are initialized to particular values when a prescaled pulse is generated, and

the state variables become initialized to the particular values also when a Power On Reset is performed.

9. (Currently amended) A device comprising:

means for receiving periodic input pulses; and

means for counting the received input pulses to generate prescaled pulses, wherein

one prescaled pulse is generated for every Qth input pulse, wherein Q is a division modulus having a value depending on a value of a modulus control signal, and

when a prescaled pulse is generated from a selected input pulse, the modulus control signal is ignored at least until <u>after</u> the onset of a next input pulse following the selected input pulse is received; and

a means for generating a reset signal in response to the prescaler receiving the Mth input pulse, wherein M is a preset integer, and

wherein a swallow counter changes the modulus control signal in response to a reset signal.

10. (Currently amended) A method comprising:

receiving periodic input pulses; and

counting the received input pulses to generate prescaled pulses, wherein

one prescaled pulse is generated for every Qth input pulse, wherein Q is a division modulus having a value depending on a value of a modulus control signal,

when the prescaled pulse is generated from a selected input pulse, the modulus control signal is ignored at least until <u>after</u> the onset of a next input pulse following the selected input pulse is received; and

generating the prescaled pulses includes:

initializing a vector of state variables when the prescaled pulse is generated, and

updating the vector during the next input pulse in a way that is indifferent to the updated modulus control signal.

11. (Original) The method of claim 10, wherein

the modulus control signal is further ignored at least until the onset of a second next input pulse following the next input pulse is received.

12. (Original) The method of claim 10, wherein

if the ignored modulus control signal acquires a different value due to the selected input pulse, the next pulse is counted according to a correspondingly different value of Q.

13. (Original) The method of claim 10, wherein

the first value of Q equals a preset number N, and

the second value of Q equals N+1.

14. (Original) The method of claim 10, wherein

when the prescaler receives an Mth one of the input pulses, the modulus control signal changes value after the prescaler has already received the onset of the next input pulse, wherein M is a preset integer.

15. (Original) The method of claim 14, further comprising:

generating a divided down signal in response to the prescaler receiving the Mth input pulse;

generating a synchronized signal in response to the divided down signal; and

generating a fast clock signal in response to the synchronized signal, and

wherein the input periodic pulses are derived from the fast clock signal.

Claim 16 (canceled).

17. (Previously Presented) The method of claim 10, wherein

the state variables are encoded in signals generated by logical devices.

18. (Previously Presented) The method of claim 10, wherein

a selected one of the state variables is set equal to one at initialization, and

the modulus control signal is ORed with the signal encoding the selected state variable.

19. (Previously Presented) The method of claim 10, wherein

if a Power On Reset is performed, the state variables are also initialized to the same states as when a prescaled pulse is generated.

20. (Previously Presented) The method of claim 10, wherein

the vector is made at least from state variables D2, D1, D0,

each of the state variables D2, D1, D0 is initialized with a value of one, and

updating the vector further includes:

generating a next D2 value derived by ORing the values of D0 and that of the modulus control signal,

generating a next D1 value derived by negative ANDing the values of D2 and D0,

generating a next D0 value derived by the value of D1, and

then using the next D2 value, next D1 value and next D0 value for updating the vector.